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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,060	03/10/2004	Tomoya Ishikawa	60188-798	4748

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/796,060	ISHIKAWA ET AL.
	Examiner	Art Unit
	Long Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *4,6 and 11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 7-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/10/04

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of specie A (Figure 1) in the reply filed on 7/8/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Note that applicant indicates that claims 1-5 and 7-10 are considered readable on the elected specie A (Figure 1). However, claim 4 does not read on the elected specie A (Figure 1) because the first circuit in Figure 1 comprises 2 NMOS transistors (M7-M8) respectively connected between the third node to ground and the fourth node to ground (i.e., the first circuit in Figure 1 does not comprise an NMOS transistor connected between <u>both</u> the third node and the fourth node and the second power supply as recited in claim 4). Thus, claim 4 does not read on the elected specie (Figure 1) so claim 4 is also withdrawn from consideration.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 9 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 9, the recitation "the first control input is controlled so that the feed-through current path is disconnected while the first input signal and the second input signal are changing" is indefinite because it is misdescriptive since it is inconsistent with what is

disclosed and shown. Note that Figure 2 of the disclosure discloses that the first control input (VS1) is controlled so that the feed-through current path is disconnected (i.e., switch-off period) after the first and second input signals are already changed (i.e., Figure 2 shows that during the switch-off period, i.e., VS1 = Lo, the first and second inputs Vin1 and Vin2 are at their respective stable state). Clarification and/or appropriate correction is requested.

With respect to claim 10, the recitation "wherein the second control input is controlled so that said second circuit fixes the voltages of the first node and the second node while the first control input is controlled so that the feed-through current path is disconnected" is indefinite because it is misdescriptive since it is inconsistent with what is disclosed and shown. Again, Figure 2 of the disclosure shows that during the first and last intervals of the switch-off period, VS2 = Hi so the second circuit (M5-M6, Figure 1) cannot fixed the voltages at the first and second node (i.e., VS2 = Hi so transistors M5 and M6 in Figure 1 should be off). Clarification and/or appropriate correction is requested.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 5 and 7-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al. (USP 6,507,224).

Note, for claims 1-3, 5, 7 and 8, Figure 2 shows a level shift circuit (110) comprising: a level shift basic circuit (96, 100, 91, 92), a first power supply (power supply), a second power supply (ground); and a control circuit (98, 102, 86, 88) including a first circuit (NMOS transistors 98 and 102) for disconnecting a feed-through current path in the level shifter circuit between the first power supply and the second power supply in response to a first control input (signal at the gates of transistors 98 and 102, note that when CLK2 = Lo, then transistors 98 and 102 are off thus disconnecting feed-through current from power supply to ground), and a second circuit (PMOS transistors 86 and 88) for fixing a voltage of an output node (OTB or OCB) from which an output signal (OTB or OCB) is output in response to a second control input (signal at the gates of PMOS transistors 86 and 88, note that when CK = Lo then transistors 86 and 88 are ON so nodes OTB and OCB are pre-charged to the power supply voltage). Note that the level shift basic circuit (96, 100, 91, 92) includes a first transistor (91), a second transistor (92), a first node (OTB), a second node (OCB), wherein at least one of the first and second nodes (OTB, OCB) is used as the output node (OTB or OCB), a third transistor (100), a third node (source of 100), a fourth transistor (96), a fourth node (source of 96), first and second input signals (OUTB, OUT). Note that, for claim 9, the recitation "the first control input is controlled so that the feed-through current path is disconnected while the first input signal and the second input signal are changing" is seen as an intended use and the circuit 110 in Figure 2 is capable of performing such intended use (i.e., by setting CLK2 = Lo while input OUT and OUTB changes (i.e., from Hi to Lo or from Lo to Hi), and set CLK2 = Hi otherwise). Note for claim 10, as discussed above

that when CLK2 = Lo then the signal at the gates of 86 and 88 is Lo so transistors 86 and 88 are ON to pre-charge the first and second nodes (OTB, OCB) to the power supply voltage while transistors 98 and 102 of the first circuit are OFF to disconnected the feed-through current path.

6. Claims 1-3 and 7-10 are also rejected under 35 U.S.C. 102(e) as being anticipated by Shimazaki et al. (USP 6,842,045).

Note, for claims 1-3 and 7-8, Figure 12 shows a level shift circuit (20) comprising: a level shift basic circuit (MN10, MN11, MN14, MN15, MP11, MP10), a first power supply (VDDH), a second power supply (ground VSSH); and a control circuit (MN16, MP12-MP13) including a first circuit (MN16) for disconnecting a feed-through current path in the level shifter circuit between the first power supply and the second power supply in response to a first control input (signal at the gate of MN16, note that when CK = Lo, then MN16 is off thus disconnecting feed-through current from VDDH to VSSH), and a second circuit (MP12-MP13) for fixing a voltage of an output node (N1 or N2) from which an output signal (N1 or N2) is output in response to a second control input (signal at the gates of MP12 and MP13, note that when CK = Lo then MP12 and MP13 are ON so node N1 and N2 is pre-charged to a fixed voltage VDDH). Note that the level shift basic circuit (MN10, MN11, MN14, MN15, MP11, MP10) includes a first transistor (MN11), a second transistor (MP10), a first node (N1), a second node (N2), wherein at least one of the first and second nodes (N1, N2) is used as the output node (N1 or N2), a third transistor (M14), a third node (source of MN14), a fourth transistor (MN15), a fourth node (source of MN15), first and second input signals (D/, D). Note that, for claim 9, the recitation "the first control input is controlled so that the feed-through current path is disconnected while the first input signal and the second input signal are changing" is seen as an intended use and the circuit

20 in Figure 12 is capable of performing such intended use (i.e., by setting CK = Lo while input D changes from Hi to Lo, and from Lo to Hi, and set CK = Hi otherwise). Note for claim 10, as discussed above that when CK = Lo then the signal at the gates of MP12 and MP13 is Lo so MP12 and MP13 are ON to pre-charge the first and second nodes (N1, N2) to fixed voltage VDDH while transistor MN16 of the first circuit is OFF to disconnected the feed-through current path.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

8/17/05

LONG NGUYEN
PRIMARY EXAMINER